L1CTT Implementation
WBS 1.2.3

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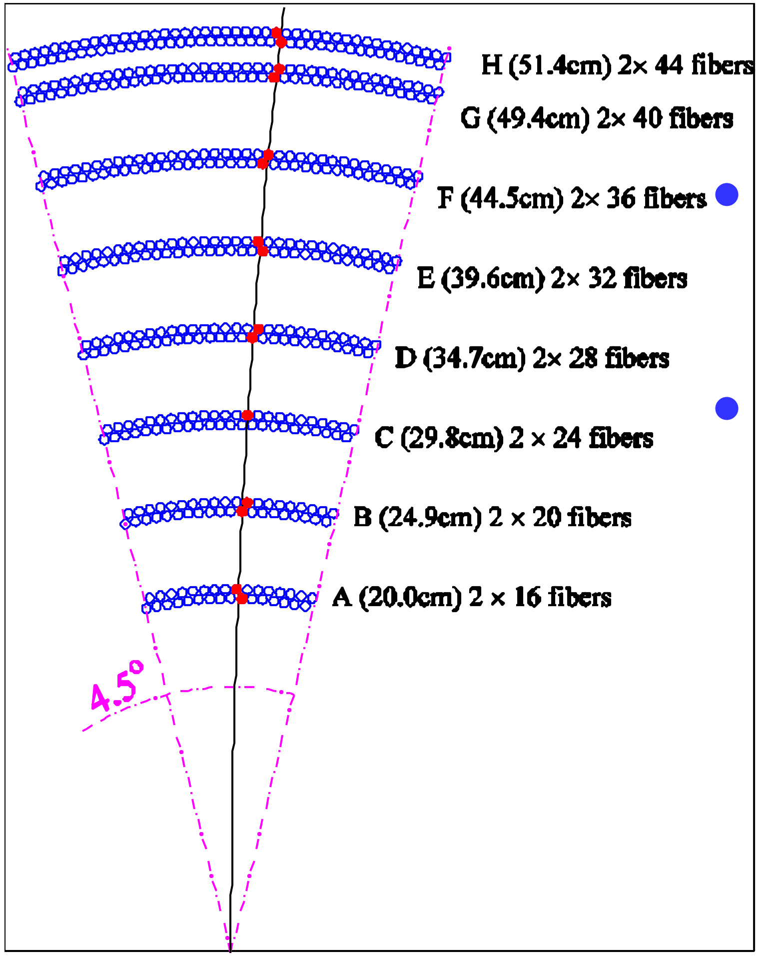
Outline:

- The Level1 Central Track Trigger System
- Implementation of RunIIa Track Trigger Logic
- Resource Evaluation for RunIIb Track Trig Logic
- RunIIb L1CTT Implementation and Design

Groups

- **Simulation and Algorithm development:**
  - **Brown:**
    - Richard Partridge
  - **Kansas:**
    - Graham Wilson
  - **Manchester:**
    - Liang Han, Terry Wyatt
  - **Notre Dame:**
    - Mike Hildredth
- **Hardware:**
  - **Boston University:**
    - Meenakshi Narain, Ulrich Heintz, Shouxiang Wu
  - **FNAL:**
    - Marvin Johnson, Jamieson Olson

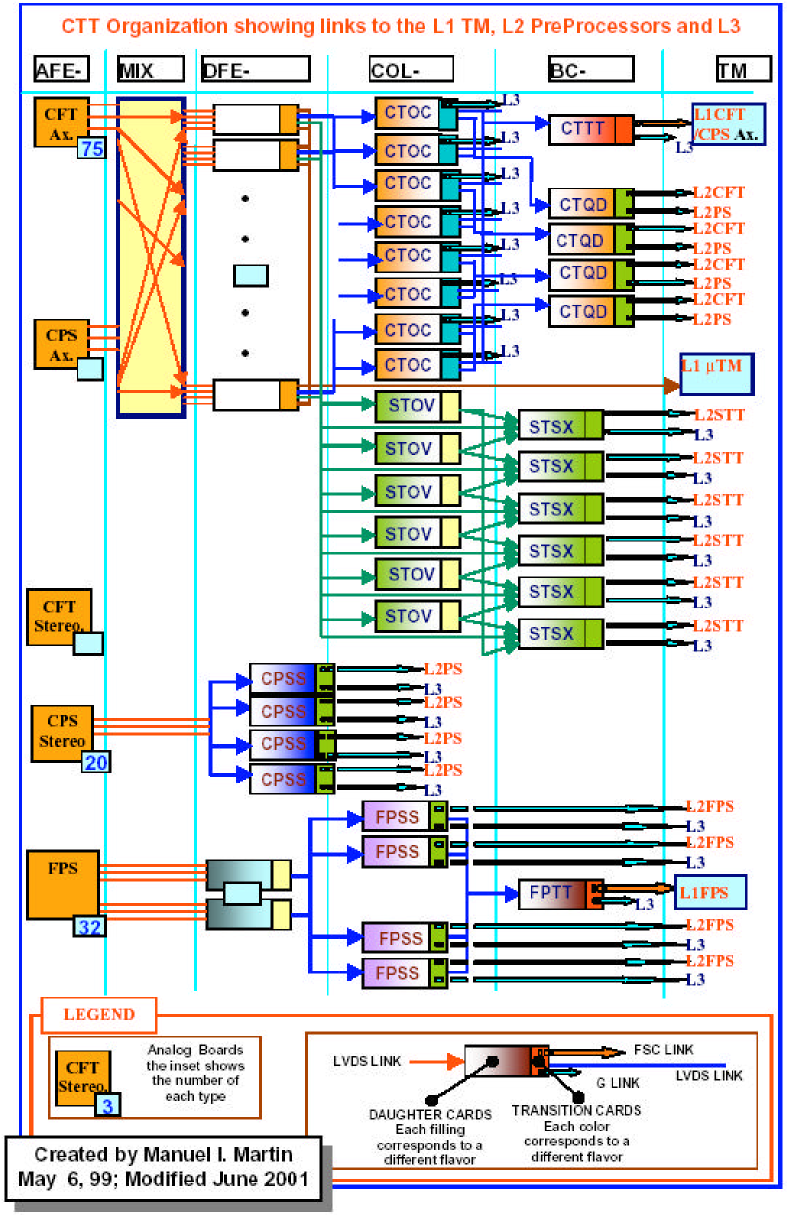
RunIIa Implementation



- Uses information from Central Fiber Tracker and preshowers
- Divide into 80 sectors (each 4.5°)
- Track Finding:
  - Define hits from using pairs of fiber in each axial layer (doublets)
  - Compare doublet hits with predefined patterns to validate a track
  - Use 4 independent pT bins (Thresholds = 1.5, 3, 5, 10)
  - Find tracks in each bin

L1CTT architecture

- **A multistage system**
  - **Analog Front End (AFE):**
    - Signals from the tracker
  - **Mixer**
    - Sort signals in trigger sector wedges
  - **Digital Front End (DFE):**
    - Track Trigger logic
  - **Collector**
    - Combine track information from several DFE boards
  - **Concentrator**
    - Construct track trigger terms
  - **Trigger Manager**
    - Construct 32 AND/OR terms used by the L1 Trigger Framework in forming the trigger decision

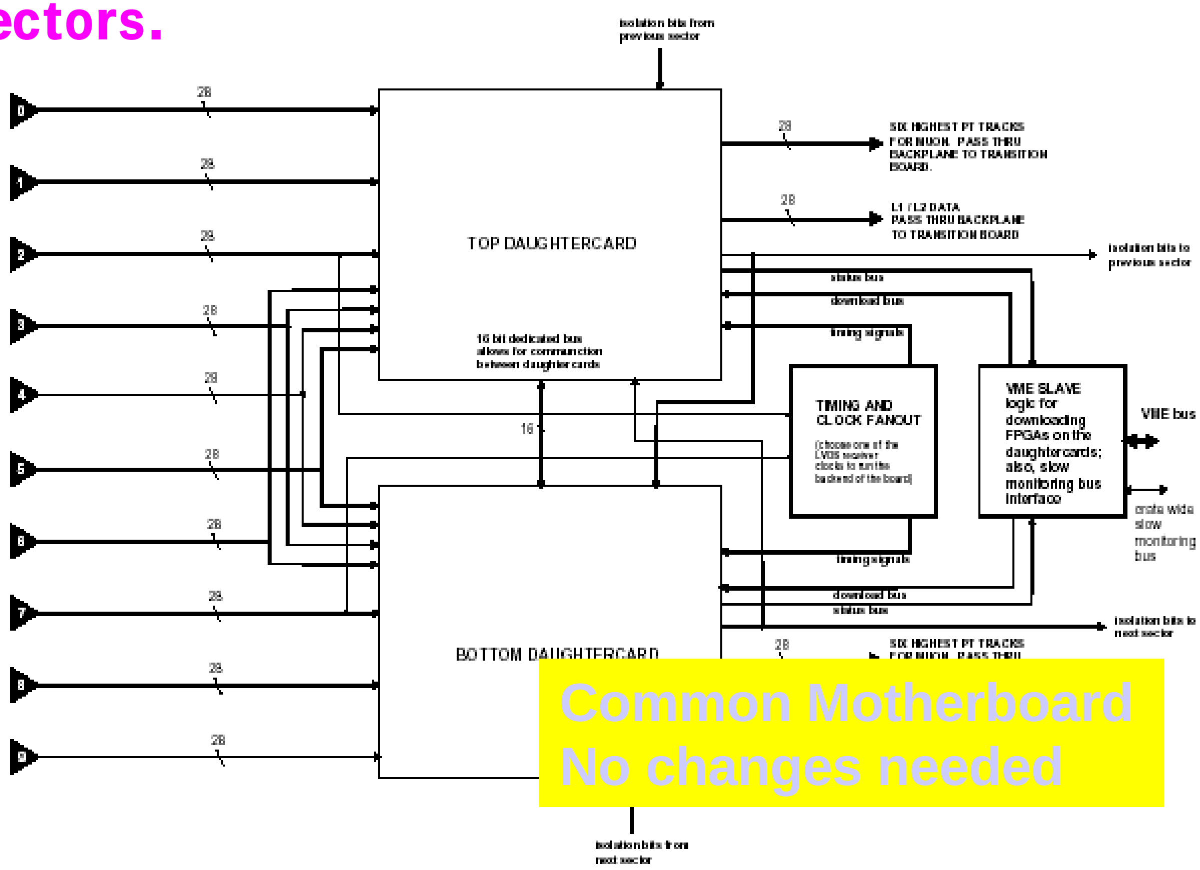


The DFEA Motherboard

- **Motherboards:**
  - general purpose, high bandwidth platform for supporting reconfigurable logic such as FPGAs.
  - A 6U x 320mm card with custom hard metric backplane connectors.

Input data on ten point-to-point LVDS links at 14.8 Gbps.

These ten links are buffered and routed to the two daughtercards.

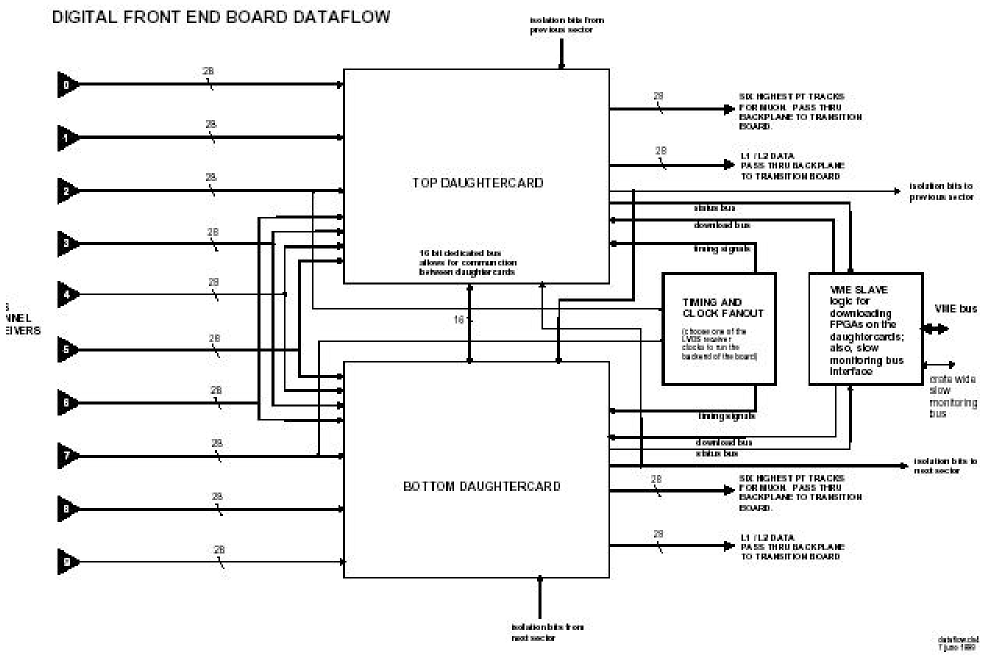


Common Motherboard
No changes needed

b

The DFEA Motherboard

- Outputs from daughterboards are fed back to the motherboard and are passed to hard metric connectors through the backplane to a transition card.
- The transition card converts the output busses back into LVDS channel links to feed the output from one DFE motherboard into a second DFE motherboard that is reconfigured as a data concentrator.

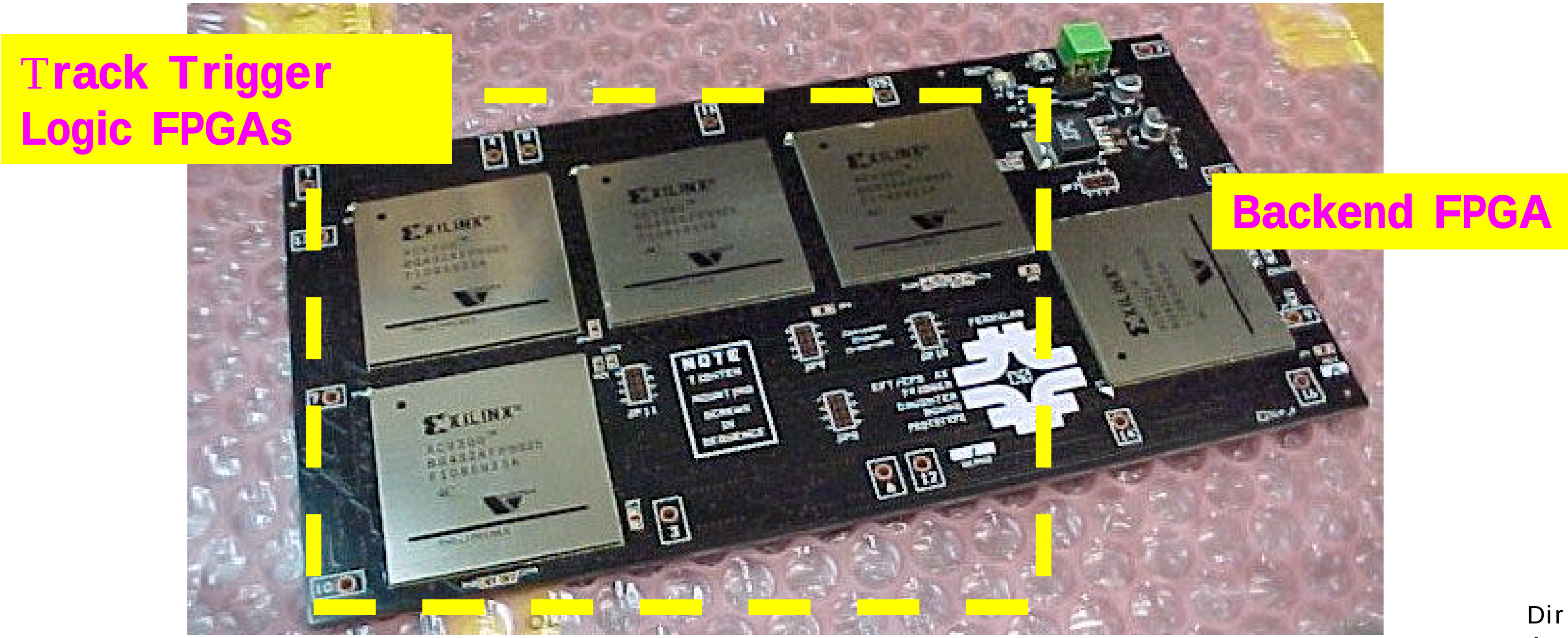


A custom high speed bus is incorporated into the DFE backplane to download configuration files at power up.

Slot 1 of the backplane is reserved for a custom DFE crate controller.

RunIIa DFEA Daughterboard

- **DFEA daughterboard:**
  - A 10-layer PC board, 7.8" x 4.125" in size.
  - Each motherboard supports 2 daughter boards.
  - 4 Track Trigger logic FPGAs (XCV series).
  - one "backend" FPGA which publishes the result.

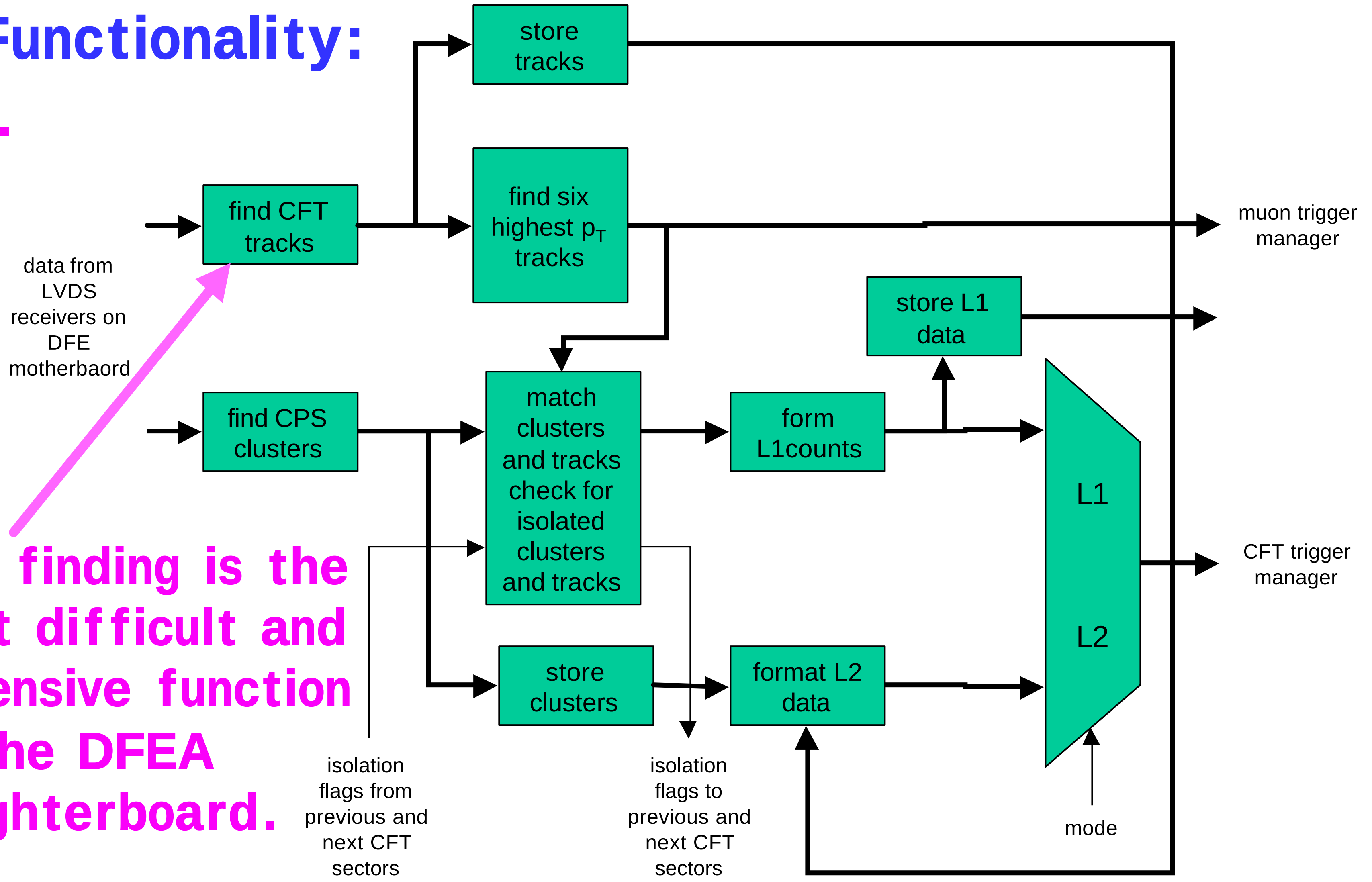


DFEA Functionality

- **Tasks of DFEA daughterboard:**
  - Find tracks in each of four pT bins
    - (Max, High, Med, and Low).
  - Find axial CPS clusters.
  - Match CPS clusters and tracks.
  - Count tracks and clusters (matched, isolated, and non isolated) for L1 readout.
  - Store tracks and clusters for L2 readout.
  - Generate a list of the six highest pT tracks to send to Muon L1

DFEA Daughterboard

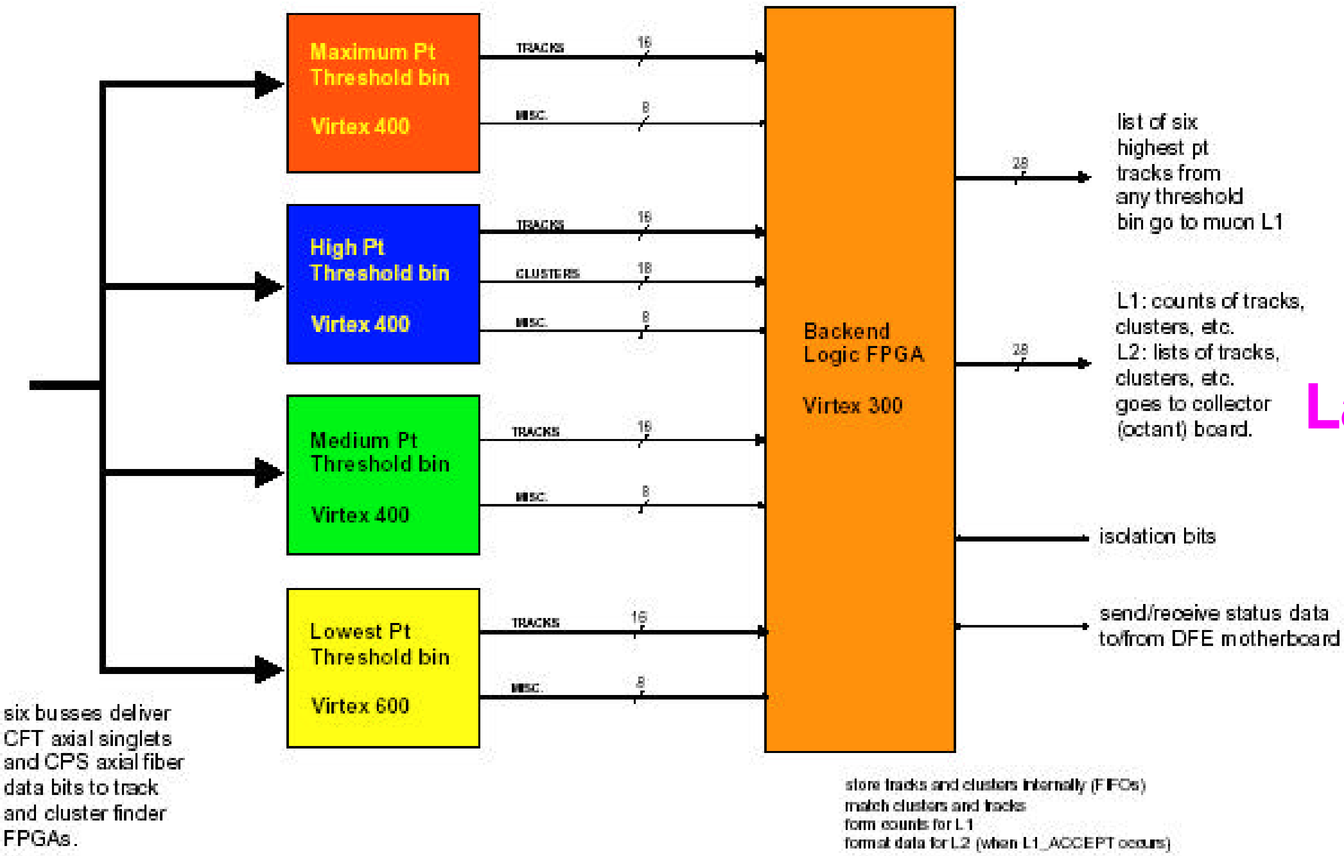
- **Functionality:**



Track finding is the most difficult and expensive function of the DFEA daughterboard.

RunIIa DFEA Dataflow

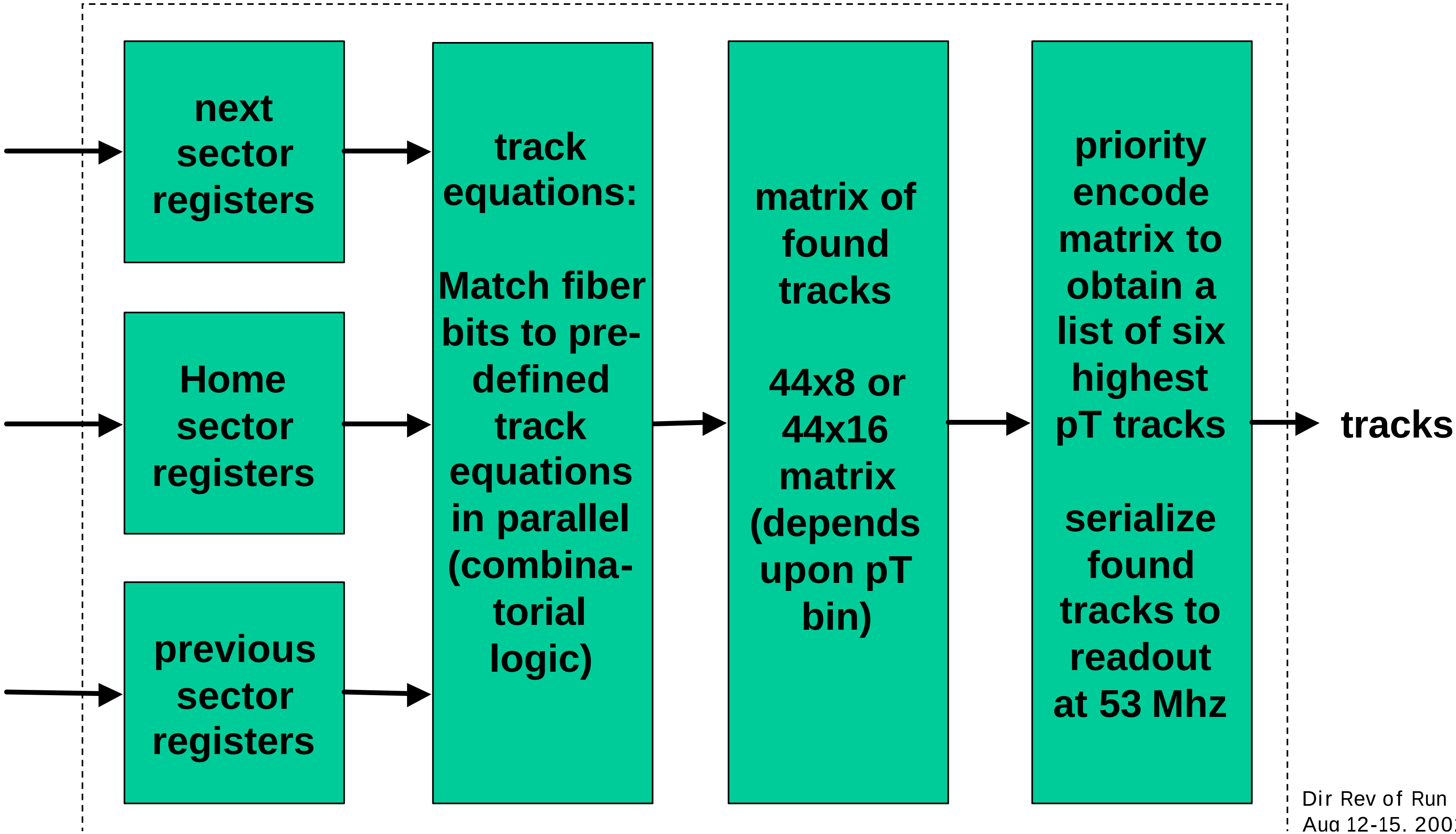
- **Dataflow Diagram and interconnections**
  - **To identify tracks down to 1.5 GeV, relatively large FPGAs must be used.**



Large number of inputs require use of Ball Grid Array packages.

Track Finder FPGA

- **Dataflow inside the Track Finder FPGA:**



RunIIb Implementation

- Use RunIIa VHDL infrastructure for RunIIb studies
- Modify the doublet former, mapping of input fiber bits and track equation logic.
- Keep input/output data paths, serialization and selection of tracks same as RunIIa.

- Implement track equations for two pT bins
  - pT > 10 GeV ("maximum")
  - 1.5 < pT < 3 GeV ("low")

Compare FPGA resources

- FPGA # Logic Cells:

RunIIa uses Xilinx Virtex series:

- XCV400 10,800 (med, lo, hi)
- XCV600 15,552 (lowest pT)

RunIIb baseline design uses Xilinx VirtexII series:

- XC2V6000 76,032

⇒Can accommodate factor of 6 – 10 more resources compared to RunIIa.

⇒Currently available product.

Resource Evaluation

- Use VirtexII series XC2V6000 chip.
- Resources Needed for pT>10 GeV bin:
  - Scheme: all 16 singlet layers (abcdefgh)
  - # of equations: 9.4k
  - # of terms per equation: 16

Number of External IOBs*	122 out of 684	17%
Number of LOCed External IOBs*	0 out of 122	0%
Number of SLICEs	**11863 out of 33792**	**35%**
*IOB = input/output block		

- Resources Needed for 1.5 < pT<3 GeV bin:
  - Scheme: inner 8 layers treated as singlets, outer 8 as doublets (abcdEFGH)
  - # of equations: 15.5k and # of terms per equation: 12
  - About 30% of XC2V6000 Chip used

The VirtexII series

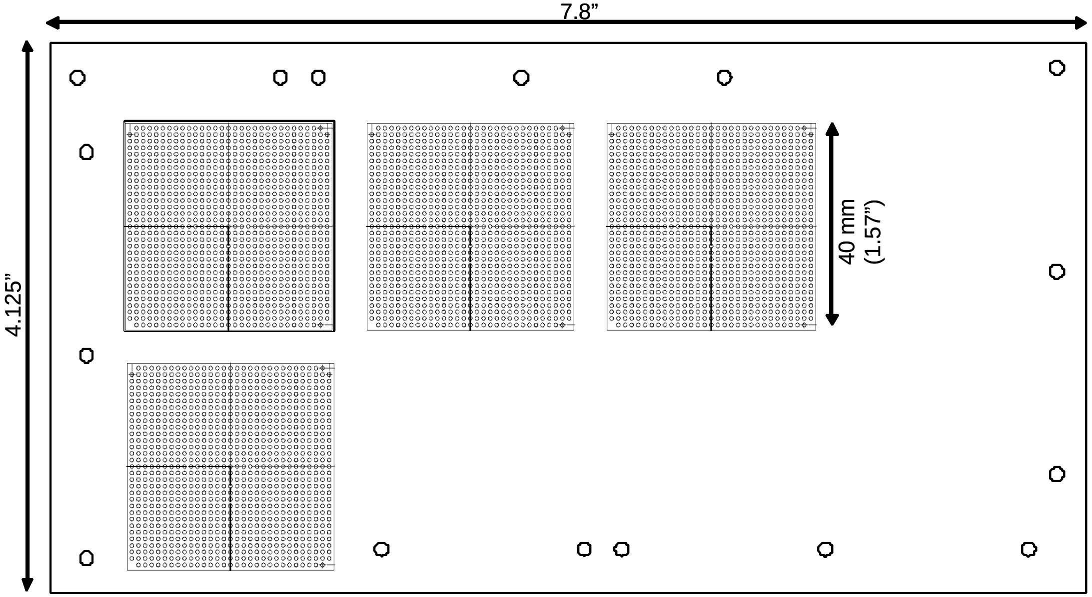
- **Virtex II FPGA specifications:**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits) Array Row x Col.	Slices	Maximum Distributed RAM Kbits	Multiplier Blocks	SelectRAM Blocks 18-Kbit Blocks	Max RAM (Kbits)	DCMs	Max I/O Pads(1)
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

RunIIb DFEA daughterboard

- Footprint of VirtexII series FPGA are different Þ new Daughter cards (DFEA).
  - Use four XC2V6000 FPGA, one for each pT bin.
  - Absorb functionality of the backend FPGA which reports the final track trigger results to the downstream boards in medium pT FPGA.

Due to the denser parts PC boards may require 2 or 4 additional layers.



- Motherboards and all other daughter boards of the L1CTT system remain the same.

Cost

item	M&S cost	contingency
firmware	$87k	$22k
prototype 1	$106k	$34k
prototype 2	$34k	$9k
production of 88 DFEA daughterboards (includes cost of XC2V chips)	$547k	$343k
installation	$2k	$0k
total	$776k	$408k

- Cost in ’02 Dollars, no escalation, no G&A

Schedule

Description of Task	Completion Date
Prototype algorithm simulated using FPGA simulation tools	1/21/2003
Algorithm coded & simulated using FPGA simulation tools	7/17/2003
Layout Prototype I boards	9/12/2003
Develop test procedures	8/28/2003
Assemble prototype I	11/14/2003
Test prototype I	2/20/2004
Layout prototype II boards	1/23/2004
Assemble prototype II	2/20/2004
Test prototype II at FNAL with the full test chain	4/16/2004
Design, Layout and Fabricate production boards	8/17/2004
Daughter boards tested and ready for installation	3/9/2005
Install and commission the trigger	6/27/05

Risk Scenarios

- 3rd prototype cycle due to:
  - PCB manufacturing problems due to 2.5 times denser and a more complicated environment.
  - Assembly problems leading to open FPGA contacts.
  - ⇒ Delay in schedule: 2 months
  - ⇒ Increased prototype costs (15k$), ~2% of project cost

- Production PCB manufacturing and assembly:
  - Faliure rate high
    - may need to salvage XC2V chips
    - May need more than 88 boards
  - Rework of FPGAs required
  - vendor may need more than 10weeks for fabrication and assembly due to the complicated nature of the boards.
  - Þ Delay in schedule: 2 months
  - Þ May want to split the order into smaller batches and proceed with testing in “parallel”.

Risk Scenarios

- Xilinx chip prices may not completely follow vendor projected quote.
- Need larger FPGA for the highest pT bin to maintain good rejection and due to equation growth due to occupancy and misalignment modeling in the CFT simulations.
  - May need 88 XC2V8000 chips

  Þ Cost increase: assigned 70% contingency